REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1, 2 and 5-30 remain pending. Claims 1, 2 and 5-30 have been rejected.

Claims 1, 15, and 23 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-2 and 5-30 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,314,546 B1 to Muddu ("Muddu") in view of U.S. Patent No. 6,601,223 B1 to Puri ("Puri").

Applicants respectfully submit that claim 1, as amended, is not obvious under 35 U.S.C. § 103(a) over Muddu in view of Puri.

The Examiner stated that "Muddu does not teach approximating by the second electrical characteristics of the test network within a specified tolerance nor creating a second graphical representation of an output of the resistive/capacitive network that approximates the first graphical representation of the output of the interconnection within a specified tolerance". (Office Action, p.4, 03/22/07).

Amended claim 1 includes the following limitations: determining a test network having second electrical characteristics that include resistive and capacitive values such that the first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network within a specified tolerance, wherein determining the test network includes adjusting the resistive and capacitive values based on the first graphical representation, wherein the determining includes creating a second graphical representation of an output of the

test network based on the resistive and capacitive values that approximates the first graphical representation of the output of the interconnection within a specified tolerance.

In contrast, neither Muddu, nor Puri, discloses such limitations of amended claim 1.

Muddu discloses a non-iterative approach for estimating interconnect capacitive effects. More specifically, Muddu discloses

> A primary approach to estimating gate delays is the modeling of admittance at the gate output. Gate delays are estimated using these models either through a delay table methodology or through an explicit simulation of the gate with the given load model.
> In accordance with an embodiment of the invention, modeling the gate load can be done by approximating an admittance of the gate load to a single capacitance model, in addition to approximating the admittance of the gate load to a Π model. After the admittance approximations, a gate response for the Π model is matched with the gate response for the single capacitance model to determine the effective capacitance.

(Muddu, col. 5, lines 12-24)(emphasis added)

Thus, Muddu merely discloses matching a gate response for one model with the gate response for the other model.

Puri, in contrast, discloses interconnect delay estimation through iterative refinement (**Figures 4 and 6**, Abstract, and col. 7, lines 57-66).

It is also respectfully submitted that Muddu does not teach or suggest a combination with Puri and that Puri does not teach or suggest a combination with Muddu. It would be impermissible hindsight based on applicants' own disclosure to incorporate the non-iterative estimation of interconnect capacitive effects of Muddu into the iterative delay estimation of Puri. Moreover, such a combination would still lack determining a test network having second electrical characteristics that include resistive and capacitive values such that the first electrical characteristics of the interconnection are approximated by the resistive and capacitive values of the test network within a specified tolerance, wherein determining the test network includes adjusting the resistive and capacitive values based on the first graphical representation, wherein the determining includes creating a second graphical representation of an output of the test

network based on the resistive and capacitive values that approximates the first graphical representation of the output of the interconnection within a specified tolerance, as recited in amended claim 1.

Given that claims 2 and 5-30 contain similar features, applicants respectfully submit that claims 2 and 5-30 are not obvious under § 103(a) over Muddu in view of Puri.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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